OIPE JC103 APR 12 2005 PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sameer P. Pendharkar	Docket No:	TI-34637
Serial No:	10/721,567	Conf. No:	5796
Examiner:	Ida M. Soward	Art Unit:	2822
Filed:	11/25/2003		
For:	DRAIN EXTENDED MOS TRANSISTOR WITH IMPROVED BREAKDOWN ROBUSTNESS		

ELECTION

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 4-8-05.

Ann Trent
Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed March 10, 2005.

Applicant hereby elects to pursue Group I of Claims 1-17, drawn to a drain-extended transistor, without traversing the Examiner's restriction requirement.

Respectfully submitted,

Peter K. McLarty
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Reg. No. 44,923

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